

What Is Claimed Is:

1. A method, comprising:
 - monitoring at least one instruction in an instruction window;
 - tracking one or more physical register references associated with one or more physical registers called on by said at least one instruction;
 - determining a reference count for said one or more physical registers based on said one or more physical register references;
 - determining a potential significance for data of said one or more physical registers based on said reference count; and
 - updating at least one register cache according to said potential significance.
2. The method of claim 1, further comprising:
 - inserting said data of said one or more physical registers into said at least one register cache according to said potential significance.
3. The method of claim 2, wherein said inserting said data is conditional on said potential significance being high.
4. The method of claim 2, wherein said inserting said data is conditional on said potential significance being low.

5. The method of claim 2, wherein said data is inserted into an empty slot in said at least one register cache.
6. The method of claim 2, further comprising:
selecting previous data from a slot in said at least one register cache according to the potential significance of said previous data; and
evicting said previous data from said slot in said at least one register cache prior to said inserting said data.
7. The method of claim 1, said tracking one or more physical register references further comprising:
associating at least one physical register identifier with said at least one instruction;
associating at least one counter with said physical register identifier; and
varying said at least one counter for each of said physical register references according to said at least one instruction.
8. The method of claim 7, wherein said at least one counter is incremented for each of said at least one physical register references.
9. An apparatus, comprising:
an instruction window of at least one instruction;

one or more physical registers to store data associated with said at least one instruction;

a counter look-up table to track one or more physical register references associated with said one or more physical registers;

a reference count circuit to determine a reference count for said one or more physical registers and a potential significance for data of said one or more physical registers based on said reference count; and

at least one register cache, wherein said reference count circuit updates said at least one register cache according to said potential significance.

10. The apparatus of claim 9, wherein said reference count circuit inserts said data of said one or more physical registers into said at least one register cache according to said potential significance.

11. The apparatus of claim 10, wherein said reference count circuit inserts said data when said potential significance is high.

12. The apparatus of claim 10, wherein said reference count circuit inserts said data when said potential significance is low.

13. The apparatus of claim 10, wherein said reference count circuit inserts said data into an empty slot in said at least one register cache.

14. The apparatus of claim 10, wherein said reference count circuit selects and evicts previous data from a slot in said at least one register cache according to a potential significance of said previous data prior to inserting said data.

15. The apparatus of claim 9, said counter look-up table further comprising:
at least one physical register identifier associated with said at least one instruction; and
at least one counter associated with said physical register identifier,
wherein said at least one counter varies for each of said physical register references according to said at least one instruction.

16. The apparatus of claim 15, wherein said counter is incremented for each of said at least one physical register references.

17. A system, comprising:
a processor including an instruction window of at least one instruction, one or more physical registers to store data associated with said at least one instruction, a counter look-up table to track one or more physical register references associated with said one or more physical registers, a reference count circuit to determine a reference count for said one or more physical registers and a potential significance for data of said one or more physical registers based on said reference count, and at least one register cache, wherein said reference count

circuit updates said at least one register cache according to said potential significance;

an interface to couple said processor to input-output devices; and

a data storage coupled to said interface to receive code from said processor.

18. The system of claim 17, wherein said reference count circuit inserts said data of said one or more physical registers into said at least one register cache according to said potential significance.

19. The system of claim 18, wherein said reference count circuit inserts said data when said potential significance is high.

20. The system of claim 18, wherein said reference count circuit inserts said data when said potential significance is low.

21. The system of claim 18, wherein said reference count circuit inserts said data into an empty slot in said at least one register cache.

22. The system of claim 18, wherein said reference count circuit selects and evicts previous data from a slot in said at least one register cache according to a potential significance of said previous data prior to inserting said data.

23. The system of claim 17, said counter look-up table further comprising:
at least one physical register identifier associated with said at least one instruction; and
at least one counter associated with said physical register identifier,
wherein said at least one counter varies for each of said physical register references according to said at least one instruction.

24. The system of claim 23, wherein said counter is incremented for each of said at least one physical register references.